WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between said plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one-end side of said plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of said main row decoder to said sub-row decoders;

wherein said plurality of sub-arrays each include said plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, said plurality of sub-arrays are arranged in said sub-word line direction, said memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion, one end of each of said memory cell blocks is coupled to a corresponding one of said bit lines, the other end thereof is connected to a corresponding one of said plate lines, a gate terminal of each cell transistor is connected to a corresponding one of said sub-word lines, said memory cell includes said cell transistor and a ferroelectric capacitor connected between source and drain terminals of said

cell transistor, and a metal interconnection used for parallel connection of said cell transistor and said ferroelectric capacitor is formed by a metal interconnection layer formed at the same level as said main-block selecting lines.

2. The semiconductor memory device according to claim 1, wherein at least part of said main block selecting lines is formed over a source, drain and gate electrode of said selection transistor.

3. The semiconductor memory device according to claim 2, wherein said selection transistor is formed by serially connecting two transistors, one of which is a transistor having a negative threshold voltage.

4. The semiconductor memory device according to claim 2, wherein said selection transistor is formed by serially connecting two transistors including a field transistor and a transistor, and a source and drain of said field transistor are connected to each other via a bottom electrode of said ferroelectric capacitor.

5. The semiconductor memory device according to claim 1, wherein said main-block selecting lines are formed by a metal interconnection layer formed at the same level as a metal interconnection connected to a top electrode of said ferroelectric capacitor.

6. The semiconductor memory device according to claim 1, wherein one or two of said main-block selecting lines are arranged for each of said memory

cell blocks in a sub-word line direction.

7. The semiconductor memory device according to claim 1, wherein memory cells arranged along adjacent bit lines are shifted by a pitch of said sub-word lines in a bit line direction and arranged.

8. The semiconductor memory device according to claim 7, wherein one or two of said main-block selecting lines are arranged for each of said memory cell blocks in said sub-word line direction.

9. A semiconductor memory device comprising:

a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between said plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one-end side of said plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of said main row decoder to said sub-row decoders;

wherein said plurality of sub-arrays each include said plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, said plurality of sub-arrays are arranged in said sub-word line direction, a metal interconnection used for forming said plate lines and a metal interconnection used for forming said main-block selecting lines are formed by metal

interconnection layers at the same level, said memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion, one end of each of said memory cell blocks is coupled to a corresponding one of said bit lines, the other end thereof is connected to a corresponding one of said plate lines, a gate terminal of each cell transistor is connected to a corresponding one of said sub-word lines, and said memory cell includes said cell transistor and a ferroelectric capacitor connected between source and drain terminals of said cell transistor.

10. The semiconductor memory device according to claim 9, wherein at least part of said main block selecting lines is formed over a source, drain and gate electrode of said selection transistor.

11. The semiconductor memory device according to claim 10, wherein said selection transistor is formed by serially connecting two transistors, one of which is a transistor having a negative threshold voltage.

12. The semiconductor memory device according to claim 10, wherein said selection transistor is formed by serially connecting two transistors including a field transistor and a transistor, and a source and drain of said field transistor are connected to each other via a bottom electrode of said ferroelectric

capacitor.

13. The semiconductor memory device according to claim 9, wherein said main-block selecting lines are formed by a metal interconnection layer formed at the same level as a metal interconnection connected to a top electrode of said ferroelectric capacitor.

14. The semiconductor memory device according to claim 9, wherein one or two of said main-block selecting lines are arranged for each of said memory cell blocks in a sub-word line direction.

15. The semiconductor memory device according to claim 9, wherein memory cells arranged along adjacent bit lines are shifted by a pitch of said sub-word lines in a bit line direction and arranged.

16. The semiconductor memory device according to claim 15, wherein one or two of said main-block selecting lines are arranged for each of said memory cell blocks in said sub-word line direction.

17. A semiconductor memory device comprising:

a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between said plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one-end side of said plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of said main row decoder to

said sub-row decoders;

wherein said plurality of sub-arrays each include said plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, said plurality of sub-arrays are arranged in said sub-word line direction, a metal interconnection used for forming said plate lines and a metal interconnection used for forming said main-block selecting lines are formed by metal interconnection layers at the same level, said memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion, one end of each of said memory cell blocks is coupled to a corresponding one of said bit lines, the other end thereof is connected to a corresponding one of said plate lines, a gate terminal of each cell transistor is connected to a corresponding one of said sub-word lines, said memory cell includes said cell transistor and a ferroelectric capacitor connected between source and drain terminals of said cell transistor, and a metal interconnection used for parallel connection of said cell transistor and said ferroelectric capacitor is formed by a metal interconnection layer formed at the same level as said plate lines and said main-block selecting lines.

18. A semiconductor memory device comprising:

a memory cell array which includes a plurality of sub-arrays, a plurality of sub-row decoders provided between said plurality of respective sub-arrays, for driving a plurality of sub-word lines, a main row decoder disposed on one-end side of said plurality of sub-arrays in a sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of said main row decoder to said sub-row decoders;

wherein said plurality of sub-arrays each include said plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, said plurality of sub-arrays are arranged in said sub-word line direction, said memory cell blocks each include a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion, one end of each of said memory cell blocks is coupled to a corresponding one of said bit lines, the other end thereof is connected to a corresponding one of said plate lines, a gate terminal of each cell transistor is connected to a corresponding one of said sub-word lines, at least part of said main-block selecting lines is formed over a source, drain and gate electrode of said selection transistor, and said memory cell includes said cell transistor and a ferroelectric capacitor connected between source

and drain terminals of said cell transistor.

19. A semiconductor memory device comprising:

a memory cell block having a plurality of series-connected memory cells and at least one selection transistor serially connected to at least one end of said series-connected portion;

wherein one end of said memory cell block on said selection transistor side is coupled to a bit line and the other end thereof is connected to a plate line, each of said memory cells includes a cell transistor and a ferroelectric capacitor connected between source and drain terminals of said cell transistor, a bottom electrode of said ferroelectric capacitor of said memory cell connected to said plate line is connected to a diffusion layer via a contact between said bottom electrode and said diffusion layer, and said diffusion layer is connected to said plate line formed of a metal interconnection layer via a contact between said diffusion layer and said metal interconnection.

20. The semiconductor memory device according to claim 19, wherein bottom electrodes of said ferroelectric capacitors of all of said memory cells contained in said memory cell block are connected to diffusion layers via only contacts between said bottom electrodes and said diffusion layers.